UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:		
Bonaventure, D. et al.	:	Group Art Unit:
	:	To Be Assigned
Serial No.:To Be Assigned	:	IPLaw T81/B503
	:	IBM Corporation
Filed: Concurrently Herewith	:	PO Box 12195
	:	RTP, NC 27709

Title: A Method For Minimizing Spill in Code Scheduled By a List Scheduler

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This Information Disclosure Statement is being submitted in connection with the above-identified application for patent. Applicants submit herewith patents, publications or other information of which they are aware, which they believe may be material to the patentability of this application and in respect of which there may be a duty to disclose in accordance with 37 C.F.R. § 1.56.

While this Information Disclosure Statement may be "material" pursuant to 37 C.F.R. § 1.56, it is not intended to constitute an admission that any patent, publication or other information referred to herein is "prior art" for this invention unless specifically designated as such.

In accordance with 37 C.F.R. § 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information as defined in 37 C.F.R. § 1.56(a) exists.

The attached form, PTO-1449, provides a listing of patents, publications, or other information as required by 37 C.F.R. § 1.98(a)(1).

Respectfully submitted,

By: _____
Gregory M. Doudnikoff, Attorney
Reg. No. 32,847

GMD/ssc
Docket:CA920030011US1
Phone: 919-254-1288 / Fax: 919-254-4330

FORM PTO-1449 (Modified)

List of Patents and Publications for
Applicant's Information Disclosure Statement

(Use several sheets if necessary)

ATTY. DOCKET NO. **CA920030011US1**

SERIAL NO. **TO BE ASSIGNED**

APPLICANT: **Bonaventure, D. et al**

FILING DATE: **To be Assigned**

GROUP: **To Be Assigned**

Reference Designation **US PATENT DOCUMENTS**

Examiner Initials		Document Number	Date	Name	Class/Subclass	Filing Date (If. Appro.)
	AA	5,819,088	10/06/98	Reinders	395/672	03/25/93
	AB	6,212,512	04/03/01	Barney, et al.	707/1	01/06/99
	AC	6,260,190	07/10/01	Ju	717/7	08/11/98

FOREIGN PATENT DOCUMENTS

	Document Number	Date	Country	Class/Subclass	Translation Yes	Translation No

OTHER ART (Including Author, Title, Data, Pertinent Pages, etc.)

AD Cheng, W. et al. "Code Generation of Nested Loops for DSP Processors with Heterogeneous Registers and Structural Pipelining" ACM Transactions on Design Automation of Electronic Systems, Vol. 4, No. 3, July 1999, pp 231-256

AE Eichenberger, A. et al. "Optimum Modulo Schedules for Minimum Register Requirements", ACM 0-89791-726/6/95/0007, pp 31-40, 1995

AF Chekuri, C. et al. "Profile-Driven Instruction Level Parallel Scheduling with Application to Super Blocks", IEEE, 1072-4451, 1996

AH Shieh, J. J. et al. "On Reordering Instruction Streams for Pipelined Computers", 22nd Annual International Workshop on Microprogramming and Microarchitecture, August, 1989

AI Shieh, J. J. et al. "Fine Grain Mapping Strategy For Multiprocessor Systems", IEEE Proceedings, Volume 138, Number 3, May, 1991

AJ Kim, B. M. et al. "Resource Allocation and Code Generation For Pointer Based Pipelined DSP Multiprocessors", IEEE, 1990

AK Aizikovitz, NE. et al. "Limiting Lifetimes of Register Sequences to Improve Register Allocation" TDB, Vol. 38, No. 11, pp 89-92

Examiner Date Considered

Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.